# Train Track Pulse Modulator

by

Tristan Grimmer and Alex Lam

Version 0.1

Supervised by: Mark Greenstreet

# Contents



# List of Figures

# 1 Introduction

This document describes the circuitry responsible for pulsing the ISD train set track. The train speed controller generates a series of pulses on a single line that represent the times at which the potential between the tracks of the train set should be zero. The pulses represent commands to each of the various trains[1]. Eight bits are sent per command, the first 4 of which are a *train address* and the second 4 the direction and speed information[2]. The Train Speed Controller is described in more detail in [MD95]. The circuitry described here treats the speed controller as a black box that simply generates pulses. The train's on-board circuitry is also treated as a black box which simply makes sense of the delivered pulses. The configuration can be seen in figure 1.

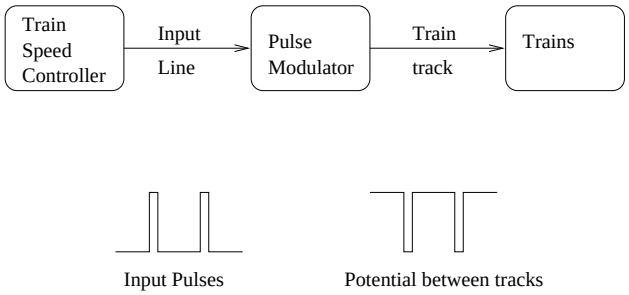


Figure 1: The Pulse Modulator in Context

The input pulse width is specified as $1ms$ with an amplitude of 5V (it is a TTL output). The inverted output, which drives the trains as well as signaling them, is not specified but should be around $16V$. The trains on board circuitry contains a rectifier that drops the track voltage before it hits the electric motor. The old design allows for a number of possible improvements. Some of it's weaker attributes are:

- It is an emitter follower configuration that uses a darlington to drive the track high. There is a voltage drop associated with this darlington which requires a higher power supply voltage. Furthermore, this transistor is being operated close to it's maximum current capability and has been known to blow.
- The transistor used to drive the track, being bipolar, is not capable of driving very many trains due to it's low continuous current rating. Three trains can be driven at the moment, which draws a maximum current of approx. $1.5A$ when all three are on their highest speed.
- The old design also uses a common ground. That is, the power supply used to drive the track is also fed through a voltage regulator and used to operate the TTL circuitry (e.g. the speed controller and train bus controller). As the track switches and trains operate there are voltage variations in the ground (with respect to the mains ground).
- The old pulse modulator, while it does have some form of short circuit protection, does not look at the input pulse to make the determination. It simply monitors the track voltage. If this voltage is *low* for too long[3] a relay is triggered that turns off the transistor base current. This is a rather brute force approach. Furthermore, a manual reset of the relay is required before each use of the train set. This 'reset' is to charge the capacitor.

The new design has avoided these shortcoming in the following ways:

- A totem pole of HEXFETs has been used as the track driving circuitry. This has a number of benefits. First, HEXFETs have a low source drain resistance (when on). The suggested FET for use in this

[1] There are 16 possible train addresses allowed using the current train speed controller.
[2] One bit for direction yielding 8 possible speeds.
[3] The length of time is controlled by a capacitor discharge.

project has a $V_{ds}$ of only $0.05\Omega$. This results in very little losses by the transistor. Second, HEXFETs are available that have high current capabilities. The suggested FET has a continuous current rating of $30A$. This is more than sufficient to run 16 trains (assuming a maximum current drain of $0.5A$ maximum per train).

- Optoisolators have been used in order to isolate the power supplies for the power track driving circuitry and the logic circuitry. This adds a degree of protection as well as noise isolation. The old circuit relies on a voltage regulator connected to a 17V supply. There is no crowbar to protect the logic circuitry if something were to go wrong with the regulator. The new design runs of an independent 5V power supply that does not have a common ground.

- Perhaps the most advanced feature is the new short circuit protection. Both the input line and the track voltage (output) are monitored at a specific sample frequency. If at any time the output is not consistent with what it should be (given the input) the HEXFETs are turned off and the track is powered down[4]. A short but sufficient cooloff time is allowed before trying to power up the track again. If the *bad* state is still present the cycle repeats. Otherwise normal operation continues. This design is, therefore, fully automatic, with both initial startup and power up/down requiring no human intervention. The parameters, such as cooloff time and sampling rate, are programmed into a PAL and are fairly easily modified.

A slightly more detailed view of the circuit can be seen in figure 2. The $100KHz$ clock is necessary as this is what the train bus clock will be operating on. This gets divided down to a reasonable sample rate. The second PAL is clocked by this rate. It looks at the input from the speed controller and the output from the voltage comparators and determines if there is a short (or other inconsistent state). It is thus able to determine what signal to send the track pulser. That is, off if there is a short, or the appropriate signal otherwise (see figure 1). The optoisolators allow different power supplies to be used and make sure that the logic circuitry is not affected by train track switch operation or train operation.

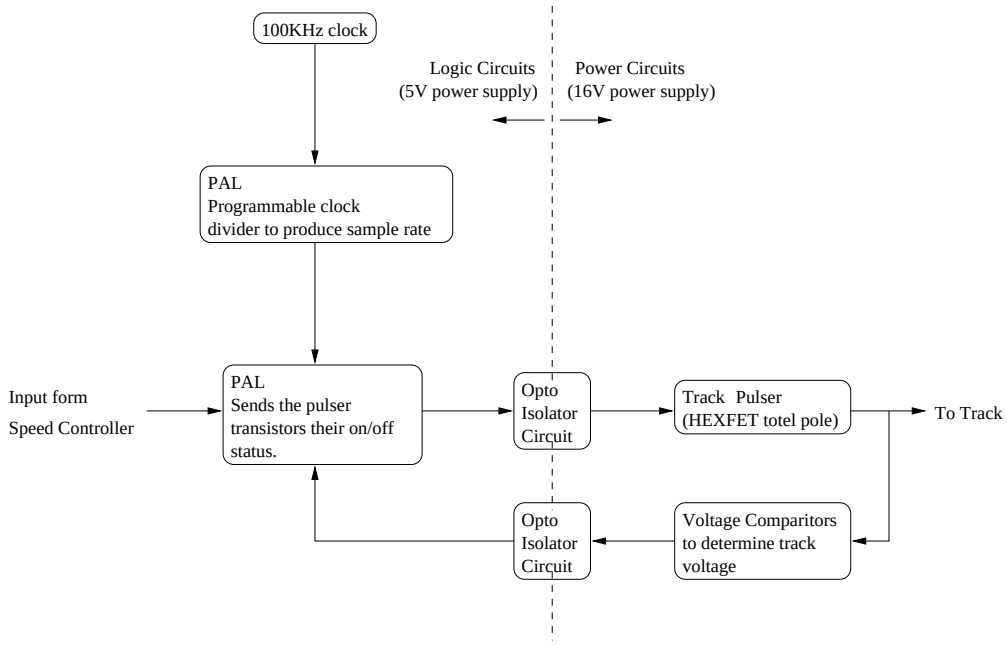


Figure 2: Pulse Modulator Block Diagram

[4] In fact a particular number of consecutive *bad* signals are required before this happens.

# 2 Design Process

The design evolved from a very modest beginning to a much more sophisticated final product. In the beginning the authors were under the false impression that FETs operated in a similar manner to JFETs and a number of incorrect designs were considered. Next a design using two N-channel HEXFETs was actually implemented. This emitter/follower design was tested to the point of being able to drive the trains. However, it was lacking a *pull-down device*. That is, it is not enough to simply kill the power to the tracks when a pulse is requested. The momentum of the electric train motors turns them into generators (non-zero back EMF) during the 'pulse' and the potential across the tracks is non-zero. This increases the possibility of an incorrect assessment by the trains on-board decoder circuitry.

A fair amount of time went into looking at the possibility of using an SCR as a pull-down device. That is, the input signal could be connected to the gate of an SCR, and the SCR would 'ground' out the track and not reset until that voltage reached zero. There were many problems with this approach however. There were timing issues (the SCR being activated earlier than the HEXFETs) as well as the problem of the SCR not resetting. The available SCRs were of the 'sensitive gate' variety and did not 'turn off' when required. This caused a continual 'grounded' state for the track, so when the input pulse went low the power being supplied to the track would be directly shorted via the SCR to the ground[5]. The SCRs were abandoned as well as the emitter/follower configuration since it required the HEXFETs to dissipate more power than is necessary. There was short circuit protection on this early model but it was of the 'capacitor discharge' variety. That is, the normal state of the capacitor was in the charged state, and if the track voltage remained low for too long it would discharge and turn off a transistor that supplied the gate voltage for the track driving transistor. This was also abandoned in favour of the following designs for the pulser and short circuit protection.

## 2.1 Track Pulser

The currently implemented track pulser circuit can be seen in figure 3.

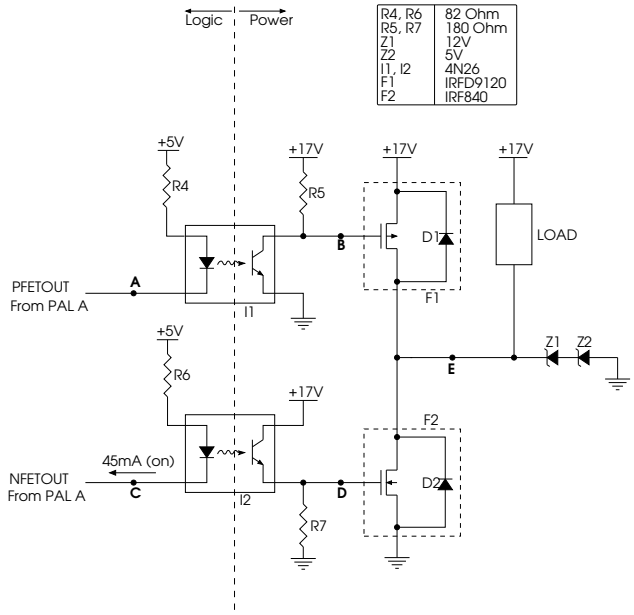


Figure 3: The HEXFET Totem Pole

[5] All of these types of experiments were conducted using a current limiting power supply and a *substitute* load. That is, a ceramic resistor.

Since the load (the trains on the track) is an inductive load the diode, **D1**, is necessary to shunt any inductive current when the PFET turns off (and the potential between the track reaches zero). As it turns out, a feature of all power MOSFETs, including the HEXFETs that are used in figure 3, is an internal reverse body-drain diode. The full schematic symbols for the HEXFETs are thus shown in dotted boxes in figure 3 and labeled **F1** and **F2**. For a more complete discussion of the HEXFETs physical construction and this integral body-drain diode see [CP93]. The electrical characteristics of this diode were not available so it was decided to add two external diodes to the actual circuit (in parallel with the internal ones). These fast switching diodes are not shown in figure 3 since when running only three trains they are not necessary. However, it is a possibility that if the load inductance increased (more trains) that they would be necessary.

As can be seen, one rail of the track is kept high while the other (E) is able to alternate between high and ground. This configuration was chosen because an N-channel HEXFET, **F2**, is able to take all the current, and N-channel HEXFETs are available with a lower $R_{ds}$ than P-channel HEXFETs. The specs for the currently used (and suggested) components are shown in the following table:

| | **Part No.** | $V_{ds}$ (V) | $R_{ds}$ ($\Omega$) | **Cont Current** (A) | **Power Disip.** (W) |
|---|---|---|---|---|---|
| N-Channel | IRF840 | 500 | 0.85 | 8.0 | 125 |
| P-Channel | IRFD9120 | -100 | 0.6 | -1.0 | 1 |
| Suggested N-Channel | IRFZ30 | 50 | 0.05 | 30 | 75 |
| Suggested N-Channel | IRFZ42 | 50 | 0.035 | 35 | 125 |
| Suggested P-Channel | IRF9Z30 | -50 | 0.14 | -18 | 74 |

Either one of the suggested N-Channel HEXFETs will do, although the higher performance IRFZ42 is slightly more expensive. There should be no problem in simply replacing the old parts as the gate threshold voltages (with respect to the source) are the same. The logical operation of the circuit can be seen in this table.

| **A** | **C** | **B** | **D** | **E** |
|---|---|---|---|---|
| Low | High | 11V | 0V | 17V |
| High | Low | 17V | 6V | 0V |
| High | High | 17V | 0V | – |

When $E$ is high there is no track potential. That is, when the input signal goes high we also want $E$ to be high. The first two rows show a consistent state, one in which the track is being pulsed and the other in which it is not. The third row shows the state the circuit is placed in when a short circuit, or otherwise inconsistent state, is detected. Both transistors are turned off. The drain voltage ($E$) will, of course, depend on whether or not there is a train on the track etc. It was decided to turn both FETs off rather than $F1$ on and $F2$ off since it protects the P-FET if the problem is not a simple short circuit[6]. The last possibility, $A$ and $C$ low, is avoided by the PAL as it would destroy both FETs. The FET gate voltages can be seen in figure 4.

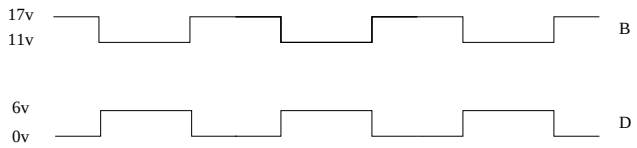


Figure 4: Fet Gate Voltages

The reason for the asymmetry in the gate driving circuits for each FET is due to the switching times of the optical isolators. For example, if $R5$ were $12K$ instead of $180\Omega$ then the voltage swing seen at B would go from 17V to virtually 0 when the optoisolator's photo-transistor was activated. It would then be possible to drive both FETs with the same signal if necessary. The problem is with the switching speed

[6] For example, if the 17V supply to the load were grounded for some reason it would blow the P-FET if it were on.

of the optoisolator when such a high resistance is used. See [OPT89] for the optoisolator characteristics. For a $12K$ resistor the rise and fall time increased to about $140\mu s$. This is too slow for the edge triggered **MC145027** decoders on board the trains. According to [CMO91] the maximum rise time for data going into the **145027** is $15\mu s$ and the maximum fall time[7] is $5\mu s$. However, as the resistance is lowered the speed of the photo-transistor increases; it's just that the photo-transistor cannot pull down as hard then. In [OPT89] resistor values as low as $10\Omega$ or $100\Omega$ are used to decrease the switching time. For this application a value of $180\Omega$ was chosen yielding an approx. $4\mu s$ rise and fall time at the gate. It should be noted that the voltage swing seen at the drain ($E$) takes only $3\mu s$ since the gate voltage must reach the threshold before the FETs will switch (see figure 6). This is within specification for the decoder. The voltage *drop* of $6V$ (down to $11V$) is easily enough to turn the P-HEXFET on. It was made sure that the optoisolator diodes were driven cleanly so $R4$ and $R6$ were chosen to produce the $45mA$ diode current (the maximum continuous current is 60mA). Of course the signal shown in figure 4 for node B cannot be used for the N-FET, so the N-FET circuit was modified to produce a $6V$ *rise* in the gate voltage from ground. This of course means that the signals at $A$ and $B$ must be the inverses of each other.

Since it is necessary to drive both FETs separately anyway (due to the short circuit protection state) this solution seems as elegant as the next from the authors point of view. Note that as a side effect, if either of the two optoisolators fail then the respective HEXFET turns off protecting it. Most other optoisolators have similar characteristics (or are even slower), the only really fast ones are for logic level outputs which will not do. Another potential solution is to add a small, fast switching, amplifier to the emitter of the photo-transistor as in figure 5, effectively turning the photo-transistor into a photo-darlington. $R3$ is necessary to increase the turn-off speed of Q2 and will probably have a value of a few thousand ohms.

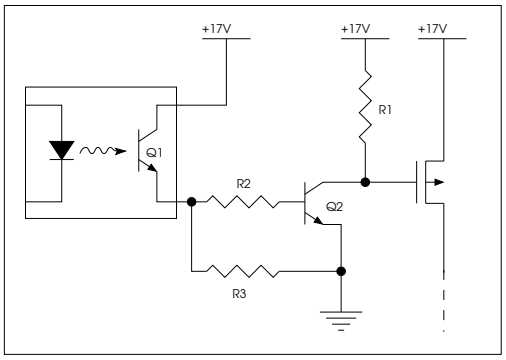


Figure 5: Another Possible Gate Driving Circuit

Even if a solution was devised that made the full gate voltage swing and could be applied to both P-Channel FET and N-Channel FET it would still be advantageous to control both independently. The reason for this is the brief short circuit current that occurs every time the gate voltage rises or falls. Figure 6 shows the 'problem'.

For the implemented circuit there will be a short circuit current for a duration of approximately $1\mu s$. The chosen HEXFETs are certainly robust enough to deal with this. A more complete discussion of this problem can be found in [Cle93] as well as some solutions. The current implementation does not address this problem. However, it allows it to be fixed by controlling each FET separately. Roughly what is desired can be seen in figure 7.

The N-Channel gate voltage must be delayed by $t_{delay}$ when a track pulse is no longer desired. At the onset of a track pulse the P-channel must be delayed. Note that this modification will also reduce voltage swing time at the drain and should be considered as a possible improvement to the circuit in the future. If a PAL is used to implement the necessary delays by 'counting' then the currently supplied 100kHz clock would not be fast enough as a minimum delay of $10\mu s$ is too long. Another alternative to introducing a faster clock

[7] See [CMO91] for their definitions of rise and fall times.

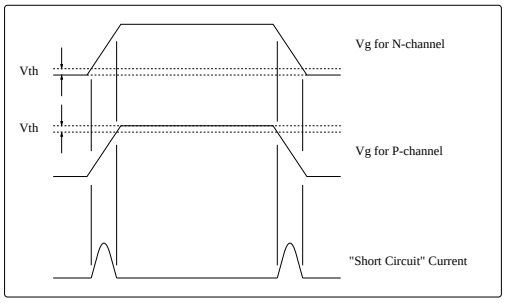


Figure 6: Brief Short Circuit Currents

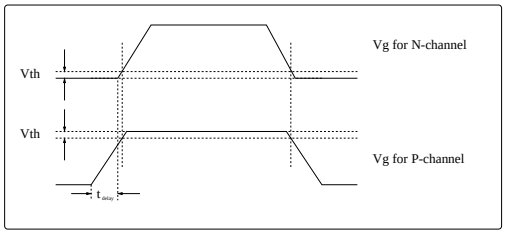


Figure 7: Eliminating the Short Circuit Current

is a 'time delay' chip which is able to delay a signal at it's input for a specified amount of time before it reaches the output. Used in conjunction with a PAL the necessary modifications should not be difficult to implement and the logic is self evident.

Another component that deserves comment is the zener diode. A 17V zener was desired but the only available components were a 5V and a 12V zener. These were put in series for an effective 17V zener. The waveforms before and after the zener were added can be seen in figure 8.

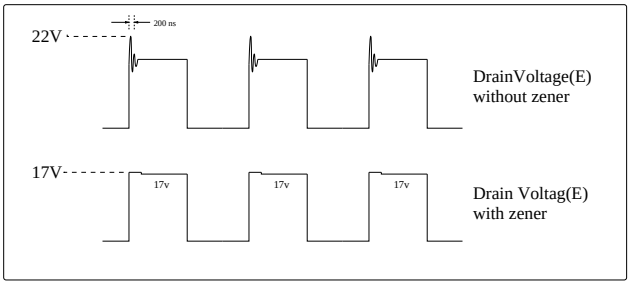


Figure 8: Voltage Spike

There was some worry that the circuit with the voltage spike might damage the **145027** decoders on the trains, so the zeners were added for protection. If the supply voltage is ever modified it is important to change the zener diode also. It should be rated at 0.2 volts higher than the power supply voltage, and of course not any less.

# 3 Short Circuit Protection

As mentioned in the introduction the short circuit protection will be automatic and not rely on any characteristics of the input pulse that should not be presumed. Having a programmable sample rate and 'false short' tolerance amount allows the circuit to be modified for a variety of conditions. For example, various numbers of trains, or different track configurations etc. The logical operation of the system can be seen in figure 9.

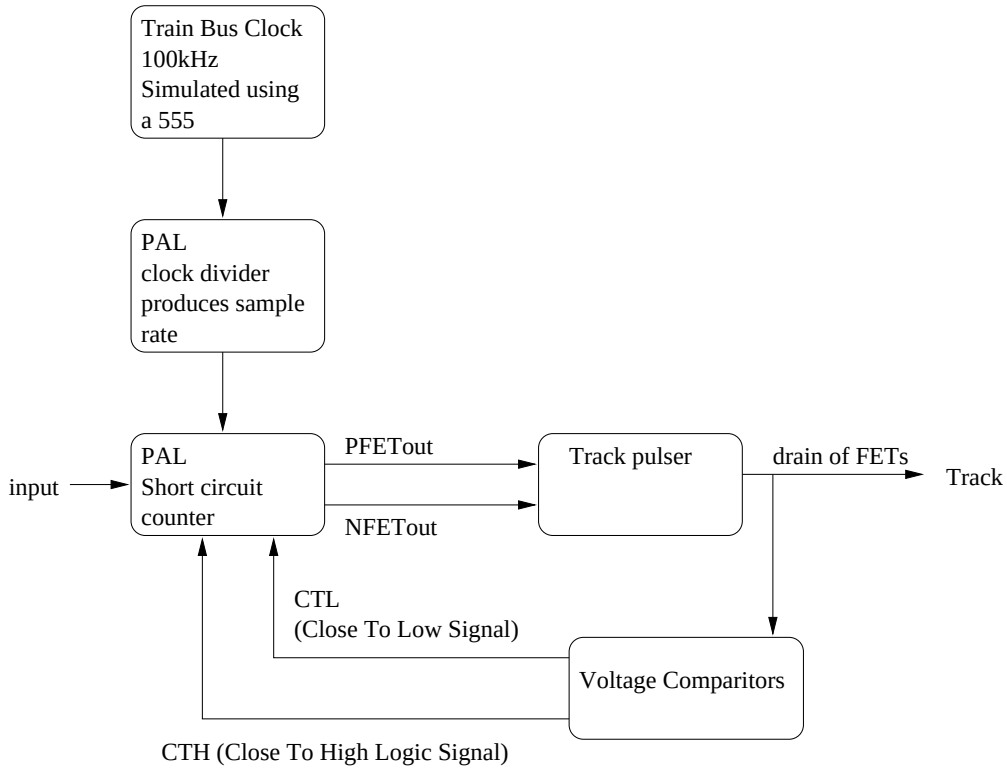


Figure 9: Short Circuit Protection Overview

The short circuit counter simply looks at the drain voltage as reported by the voltage comparators. If this voltage is not at what it should be given the current input it increments a counter. When this counter reaches a certain threshold it sets the 'mode' to off. The input signal is always 'anded' with the mode to determine the values of the NFETout and PFETout outputs. If there is an inconsistent state for long enough and the mode is off the counter continues counting to an upper bound (the cool-off time). When this is reached the mode gets set to 'on' again to see if the short is still present. Here is a description of each component of the S/C protection circuitry.

## 3.1 Voltage Comparators

Figure 10 shows the two comparators.

They are standard low voltage comparators using LM3900 amplifiers as described in [OPE93]. The reference voltages are connected to the non-inverting inputs of A1 and A2. The choices for R9, R10, and R11 determine what these reference voltages are. The chosen reference voltages are $14.8V$ and $2.2V$ respectively for A1 and A2. Since these values are easily and accurately determinable the circuitry would be easily modifiable to handle situations in which the drain voltage did not swing all the way from 0 to 17V. Perhaps a future improvement to the trains would allow them to detect a much milder voltage drop. The

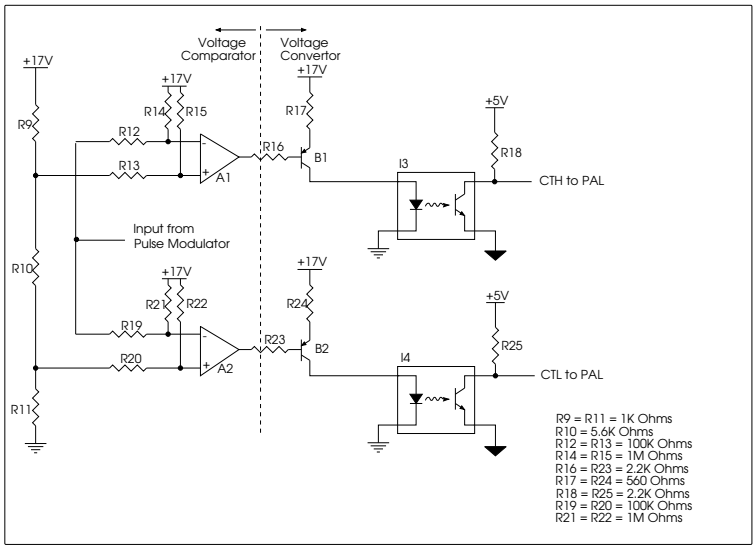


Figure 10: Voltage Measurements at the Drain

output of the amplifiers is again amplified by B1 and B2. The amplifiers could have driven the optoisolators directly but 'over driving' the inverting input would be necessary to achieve the required current in the optoisolators (see [OPE93]). This 'over driving' would mean that the voltage swing of the output would occur over a several volt difference between the amplifier inputs[8]. The bipolars allow a 20mA diode current and a full voltage swing over a 0.1V difference in the inputs. Note that the CTH and CTL (close to high and close to low) are negative logic.

## 3.2 Clock

Since the new train bus is not built yet the 100Khz clock rate was generated using a 555 as in figure 11.

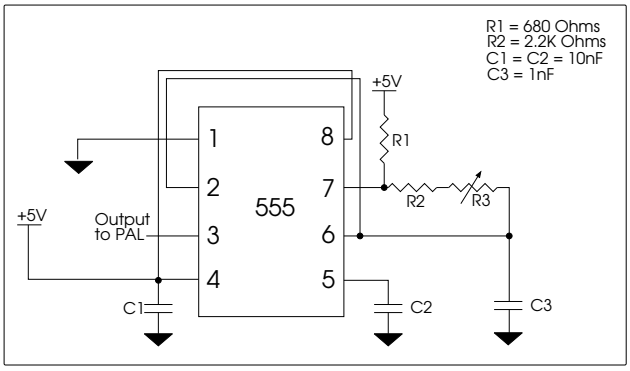


Figure 11: 100Khz Clock

$R2$ was chosen large so that something close to a 50% duty cycle could be achieved. $R3$ allows an exact frequency adjustment. As a reminder the time spent low and high are given by the following.

[8] For a 10mA diode current the difference between the amp inputs was up to 2.5V.

$$t_h = 0.693(R_1 + R_2)C_3$$
$$t_l = 0.693 R_2 C_3$$

### 3.3 PAL Programming

Two CE22V10H PALs are used although the functionality is not divided as in figure[9] 9. A block diagram of the functionality of each PAL can be seen in figures 12 and 13.

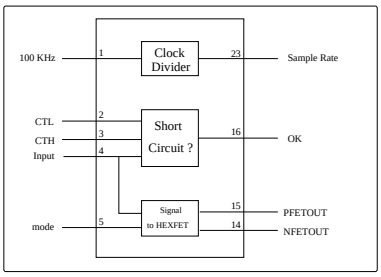


Figure 12: PAL A

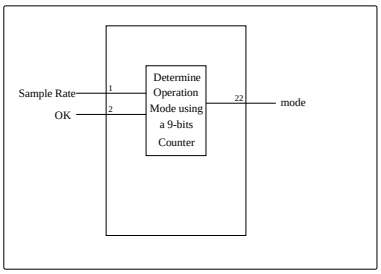


Figure 13: PAL B

The ST code for the clock divider and the mode determination PAL can be seen in Appendix A. The operation has been described in enough detail that the code should be fairly self explanatory. The ABEL code used to program the PALs is given in Appendix B. The short circuit determination and the 'signal to HEXFET' box are both combinational circuits. The previously suggested modification to reduce the brief short circuit current would require a modification to the 'signal to HEXFET' box. As both PALs are currently full a third would have to be introduced as well as the time delay chip. It should be noted that the 'Short Circuit' detection box is slightly misnamed since it outputs whether the system is in an **OK** state. Other problems with the circuit would cause **OK** to be false, such as a failure of any of the four optoisolators or amplifiers. This is slightly more general than just checking if the conditions necessary for a short are present. Finally the complete system can be constructed.

# 4 The Complete System

Putting all of the parts together yields the schematic in figure 14.
The LED goes on when the MODE is low (i.e. when there is a short or other problem).

[9] Originally the functionality was divided in such a way but only a six bit counter was possible for the short circuit counter. By dividing the tasks a 9 bit counter was achievable.

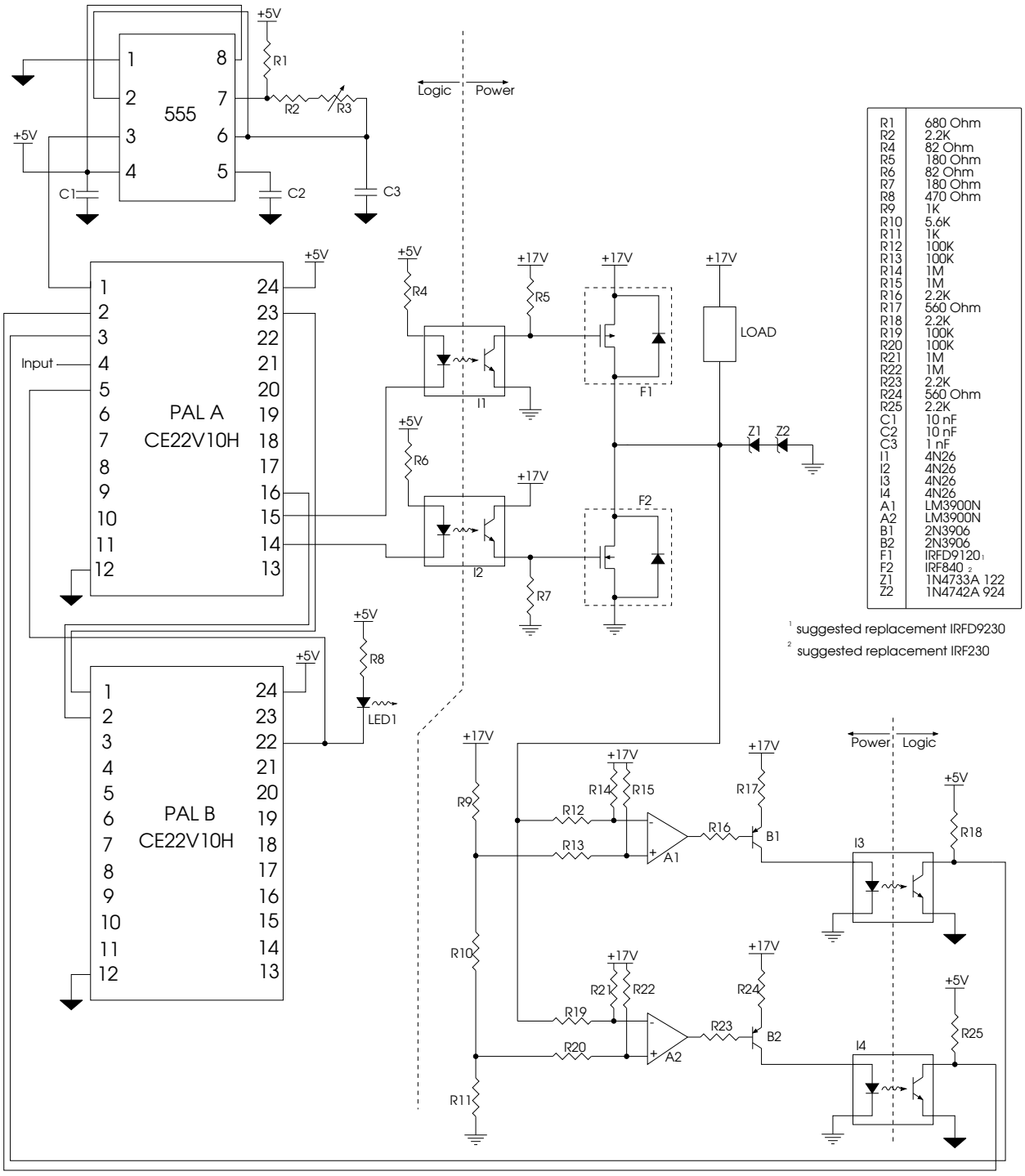


Figure 14: Complete Schematic

## 4.1 Trial Run

The system was tested with two trains[10]. The number of consecutive 'not **OK**' readings before switch-off was set to 8 (i.e. maxsamp = 8). The sample rate was set to once every $200\mu s$ (i.e. divisor = 10) and the cool-off time for the N-Channel HEXFET to $101600\mu s$ (i.e. cooldown = 500). This worked fine for two trains. A short circuit would only keep the N-Channel HEXFET warm. The trains were run for 20 minutes before one of them derailed[11].

## 4.2 Possible Modifications

To end, here is a list of possible/suggested improvements and changes to the system that may be required.

- **Regulated Power Supply:** Currently the 17V power supply is unregulated and is known to fluctuate.
- **Separate Logic Power Supply:** Currently the 17V power supply has a voltage regulator attached which supplies the power for the train bus logic circuits. All the logic circuitry should be on a separate supply (There is also no crowbar to protect the logic circuitry.)
- **Optoisolators for the Track Switch Circuitry:** Currently the track switch circuit shares a common ground with the 17V power supply. This circuit should also be isolated.
- **Zener Diodes:** If the track power supply is modified the zeners must be made to match (+ 0.2 V).
- **More Trains:** It may be necessary to modify the values for the sample rate, number of allowed consecutive shorts, and cool-down period when more trains are added to the system. A heat sink may also be necessary on the N-Channel HEXFET if more trains are run.
- **Brief Short Circuit:** The short circuit through the totem pole could be fixed as described previously.
- **HEXFET Gate Driving Circuit:** If desired the gate driving circuitry could be modified as previously suggested.
- **Smaller $\Delta V$ Necessary for Pulse Determination:** The trains could be modified to 'see' a smaller change in the track voltage as a pulse. This change would require a slight modification to the comparator circuit as described above. It would also require a slight modification to the pulse driver circuitry (the source of the N-Channel HEXFET would no longer be connected to ground, but rather to a higher voltage).

[10] The third train was out of commission at the time of the writing.
[11] And successfully activated the S/C protection.

# 5 Appendix A: ST code

ST code is available for both the clock divider and the short circuit protection. The PALs, however, also have some combinational code that is too trivial to be written in ST.

clockdiv.std

```
(*************************************************************)
(* Train Speed Controller Clock Divider                      *)
(* Date: December, 1995                                      *)
(* Alex Lam   and   Tristan Grimmer                          *)
(*************************************************************)

DEFINITION MODULE clockdiv;
  EXPORT clk;

  TYPE clock = CELL(STATIC divisor:  INTEGER);
  (* import clock divisor *)
  (* note that the supplied value should be one half the *)
  (* actually desired divisor *)
  STATIC clk: clock;
END.
```

clockdiv.sti

```
(*************************************************************)
(* Train Speed Controller Clock Divider                      *)
(* Date: December, 1995                                      *)
(* Alex Lam   and   Tristan Grimmer                          *)
(*************************************************************)

IMPLEMENTATION MODULE clockdiv;

  FROM stringIO IMPORT WriteString;
  FROM strings IMPORT IntToString;
  FROM strings IMPORT BoolToString;
  STATIC
    clk: clock =
  STATE
    count, resetcount : INTEGER = 0, divisor;
    output :BOOLEAN = TRUE;
  BEGIN
    << count := (count + 1) MOD resetcount >> +
    << (count = resetcount-1 ) -> output := NOT output >> +
    WriteString(BEGIN BoolToString(output,FALSE)  END)

  END; (* clk *)

END. (* module *)
```

scpal.std

```
(*************************************************************)
(* Train Speed Controller Short Circuit PAL                  *)
(* Date: December, 1995                                      *)
(* Alex Lam   and   Tristan Grimmer                          *)
(*************************************************************)

DEFINITION MODULE scpal;
  EXPORT sc, tester;
  (* Import Cool-off FET time *)
  TYPE
    tst = CELL(STATIC CoolOff, MaxSamples: INTEGER);
    shrtcirc = CELL(short, mode: BOOLEAN;
                    count,cooldown,maxsamp :INTEGER);
  STATIC
    sc: shrtcirc;
    tester: tst;
END.
```

scpal.sti

```
(*************************************************************)
(* Train Speed Controller Short Circuit PAL                  *)
(* Date: December, 1995                                      *)
(* Alex Lam   and   Tristan Grimmer                          *)
(*************************************************************)

IMPLEMENTATION MODULE scpal;

  FROM stringIO IMPORT WriteString;
  FROM strings IMPORT IntToString;
  FROM strings IMPORT BoolToString;
  IMPORT con;

  STATIC
    sc: shrtcirc =
  BEGIN
    << mode AND short -> count := count + 1 >>
    << mode AND (count = maxsamp) -> mode := FALSE >> +
    << mode AND NOT short -> count := 0 >> +
    << NOT mode ->   count := (count + 1) MOD cooldown >> +
    << NOT mode AND (count = cooldown - 1) -> mode := TRUE >>
  END; (* sc *)

  STATIC
    tester: tst =
      STATE
        short, mode : BOOLEAN = FALSE, FALSE;
        count, cooldown, maxsamp  : INTEGER = 0, CoolOff, MaxSamples;
      TYPE S = FUNCTION(s: BOOLEAN; c: INTEGER; m: BOOLEAN): STRING;
      STATIC stringify: S =
      BEGIN
        con.cat5( BoolToString(s,FALSE), "  ",
                  IntToString(c, 10), "  ",
                  BoolToString(m,FALSE))
      END;

    BEGIN
      (
         << short := TRUE >>      (* simulates operation *)
       || << short := FALSE >>
      ) +
      sc(short, mode, count, cooldown, maxsamp) +
      WriteString(BEGIN stringify(short, count, mode) END)
    END;  (* tester *)


END. (* module *)
```

# 6 Appendix B: ABEL code

ABEL code is available for both PALs. The conversion from the applicable ST code to abel is fairly straightforward. However, there is no 'MOD' operator in ABEL that can be applied to sets (such as the counter) so a slight modification was necessary (see the comment in clock2.abl). It was also noticed that for correct operation only one **WHEN** form is allowed per registered variable. That is, the '**WHEN ... THEN ... ELSE WHEN ... THEN ... ELSE ...**' format is necessary. The last slight difference is the use of the combinational 'OK' variable in the scpal2.abl file. In the ST code it was negative logic and was called 'short'.

clock2.abl

```
"************************************************************
"* PAL A ABEL Code                                          *
"* Date: December, 1995                                     *
"* Alex Lam   and   Tristan Grimmer                         *
"************************************************************
Module clock2

Declarations
        clock2 DEVICE 'p22v10';

        clockin PIN 1;
        clockout PIN 23 ISTYPE 'reg';
        C0,C1,C2,C3,C4,C5 PIN 17,18,19,20,21,22 ISTYPE 'reg';
        counter = [C5,C4,C3,C2,C1,C0];

        divisor = 10;  "Value may require modification

        VCG,!VCH,input,ok PIN 2,3,4,16 ISTYPE 'com';

        mode,!PFETout,NFETout PIN 5,15,14 ISTYPE 'com';
        HIGH = 1;
        LOW = 0;


Equations
        counter.clk = clockin;
        clockout.clk = clockin;

        "Implements (counter++ MOD divisor)
        WHEN (counter == (divisor - 1)) THEN
          counter := 0;
        ELSE
          counter := counter + 1;

        WHEN (counter == (divisor - 1)) THEN
          clockout := !clockout;
        ELSE
          clockout := clockout;

        ok = (input $ VCG) & (VCG $ VCH);

        WHEN mode THEN
           NFETout = input;
        ELSE
           NFETout = HIGH;

        WHEN mode THEN
           PFETout = input;
        ELSE
           PFETout = LOW;

End clock2
```

scpal2.abl

```
"************************************************************
"* PAL B ABEL Code                                          *
"* Date: December, 1995                                     *
"* Alex Lam   and   Tristan Grimmer                         *
"************************************************************
Module scpal2

Declarations
        scpal2 DEVICE 'p22v10';
        sampleclock PIN 1;
        ok PIN 2 ISTYPE 'com';
        mode,C0,C1,C2,C3,C4,C5,C6,C7,C8
          PIN 14,15,16,17,18,19,20,21,22,23 ISTYPE 'reg';
        counter = [C8,C7,C6,C5,C4,C3,C2,C1,C0];
        maxsamp = 8;        "Maximum number of not OK's before shutdown
        cooldown = 500;     "Number of cycles before startup again
        ON = 1;
        OFF = 0;

Equations
        counter.clk = sampleclock;
        mode.clk = sampleclock;

        WHEN (mode & (counter == maxsamp)) THEN
          mode := OFF;
        ELSE WHEN (!mode & (counter == (cooldown - 1))) THEN
          mode := ON;
        ELSE
          mode := mode;

        WHEN (mode & !ok) THEN
          counter := counter + 1;
        ELSE WHEN (mode & ok) THEN
          counter := 0;
        ELSE WHEN (!mode & (counter == (cooldown - 1))) THEN
          counter := 0;
        ELSE WHEN (!mode) THEN
          counter := counter + 1;
        ELSE
          counter := counter;

End scpal2
```

# 7 Data Books and Other References

This section is supplied so that the exact specifications for any of the components in this design can be easily obtained. The most informative reference on the train hardware in general is probably Andrew Martin. However, these data books were also helpful.

# References


[Cle93] S. Clemente. An Introduction to International Rectifier P-Channel HEXFETs. In *HEXFET Power MOSFET Designer's Manual.* pages 27-31, 1993, International Rectifier.

[CMO91] *CMOS Application-Specific Standard ICs.* pages 6-17 to 6-24, 1991, Motorola.

[CP93] S. Clemente and B. Pelly. A Chopper for Motor Speed Control Using Parallel Connected Power HEXFETs. In *HEXFET Power MOSFET Designer's Manual.* pages 33-44, 1993, International Rectifier.

[HH89] Paul Horowitz and Winfield Hill. *The Art of Electronics.* 1989, Cambridge University Press.

[MD95] Joanna McGrenere and Mohammad Darwish. *Train Set Speed Controller version 0.1.* 1995, ISD Group, CS, UBC.

[OPE93] *Operational Amplifier Databook.* 1993, National Semiconductor.

[OPT89] *Optoelectronics Device Data.* pages 6-2 to 6-5, 1989, Motorola.